signal responsive to a global data strobe signal until a write control signal is generated. The data strobe signals are used to store respective samples of a data signal in respective storage devices so that data signal samples obtained responsive to the first data strobe signals are overwritten with data signal samples obtained responsive to subsequent data strobe signals. When the write control signal is generated, the first data strobe signals are no longer generated responsive to the global data strobe signals. As a result, a data signal sample last obtained prior to the write control signal being generated is saved and a data signal sample obtained after the write control signal is saved.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a logic diagram a data strobe circuit and method according to one embodiment of the invention.

Figure 2 is a logic diagram of one embodiment of a logic circuit used in the data strobe circuit of Figure 1.

Figures 3A-J are timing diagrams showing various signals present in the data strobe circuit of Figure 1.

Figure 4 is a block diagram of one embodiment of a memory device using the data strobe circuit of Figure 1.

Figure 5 is a block diagram of one embodiment of a computer system using the memory device of Figure 4.

DETAILED DESCRIPTION OF THE INVENTION

One embodiment of a data strobe circuit 10 that is insensitive to noise on data strobe lines and thus captures write data responsive only to valid data strobes is shown in Figure 1. As explained more fully below, the circuit 10 operates by strobing data on each transition of a DS pulse on a data strobe DS line, saving the data strobed on the last two transitions prior to a predetermined write command, and saving the data strobed on the first two transitions following the predetermined write command. As a result, any data strobed by noise signals in the preamble are overwritten with correctly strobed data.